**DAILY ASSESSMENT FORMAT**

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| **Date:** | **01 June 2020** | **Name:** | **Veronica gudagur** |
| **Course:** | **HDL design** | **USN:** | **4al16ec091** |
| **Topic:** | **Industry Applications of FPGA**  **FPGA vs ASIC Design Flow** | **Semester & Section:** | **8-B** |
| **Github Repository:** | **Veronica-g** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report**  **FPGA:**  An FPGA is a (mostly) digital, (re-)configurable ASIC.  It is say mostly because there are analog and mixed-signal aspects to modern FPGAs.  For example, some have A/D converters and PLLs.  I put re- in parenthesis because there are actually one-time-programmable FPGAs, where once you configure them, that’s it, never again.  However, most FPGAs you’ll come across are going to be re-configurable.  FPGA-basics-gates   1. **Parallel processes** – if you need to process several input channels of information (e.g. many simultaneous A/D channels) or control several channels at once (e.g. several PID loops). 2. **High data-to-clock-rate-ratio** – if you’ve got lots of calculations that need to be executed over and over and over again, essentially continuously. The advantage is that you’re not tying up a centralized processor. Each function can operate on its own. 3. **Large quantities of deterministic I/O** – the amount of determinism that you can achieve with an FPGA will usually far surpass that of a typical sequential processor. If there are too many operations within your required loop rate on a sequential processor, you may not even have enough time to close the loop to update all of the I/O within the allotted time. 4. **Signal processing** – includes algorithms such as digital filtering, demodulation, detection algorithms, frequency domain processing, and image processing, or control algorithms.   In the case of FPGAs, the following are generally the main disadvantages of FPGA-based solutions.   1. **Complex calculations infrequently** – If the majority of your algorithms only need to make a computation less than 1% of the time, you’ve generally still allocated those logic resources for a particular function (there are exceptions to this), so they’re still sitting there on your FPGA, not doing anything useful for a significant amount of time. 2. **Sorting/searching** – this really falls into the category of a sequential process. There are algorithms that attempt to reduce the number of computations involved, but in general, this is a sequential process that doesn’t easily lend itself to efficient use of parallel logical resources. Check out the sorting section [here](http://bigocheatsheet.com/) and check out this article [here](http://www.embedded.com/design/configurable-systems/4006440/Sorting-data-in-two-clock-cycles) for some more info. 3. **Floating point arithmetic** – historically, the basic arithmetic elements within an FPGA have been fixed-point binary elements at their core. In some cases, floating point math can be achieved (see [Xilinx FP Operator](http://www.xilinx.com/products/intellectual-property/floating_pt.html) and [Altera FP White Paper](https://www.altera.com/en_US/pdfs/literature/wp/wp-01028.pdf) ), but it will chew up a lot of logical resources. Be mindful of single-precision vs double-precision, as well as deviations from standards. However, this FPGA weakness appears to be starting to fade, as hardened floating-point DSP blocks are starting to be embedded within some FPGAs (see [Altera Arria 10 Hard Floating Point DSP Block](https://www.altera.com/products/fpga/features/dsp/arria10-dsp-block.html)). 4. **Very low power** – Some FPGAs have low power modes (hibernate and/or suspend) to help reduce current consumption, and some may require external mode control ICs to get the most out of this. Check out an example low power mode FPGA [here](http://www.xilinx.com/support/documentation/application_notes/xapp480.pdf). There are both static and dynamic aspects to power consumption. Check out these [power estimation spreadsheets](https://www.xilinx.com/products/technology/power/xpe.html) to start to get a sense of power utilization under various conditions. However, if low power is critical, you can generally do better power-wise with low-power architected microprocessors or microcontrollers. 5. **Very low cost** – while FPGA costs have come down drastically over the last decade or so, they are still generally more expensive than sequential processors.   ASIC stands for Application Specific Integrated Circuit. As the name implies, ASICs are application specific. They are designed for one sole purpose and they function the same their whole operating life. For example, the CPU inside your phone is an ASIC. It is meant to function as a CPU for its whole life. Its logic function cannot be changed to anything else because its digital circuitry is made up of permanently connected gates and flip-flops in silicon. The logic function of ASIC is specified in a similar way as in the case of FPGAs, using hardware description languages such as Verilog or VHDL.   |  |  | | --- | --- | | FPGA v/s ASIC | parameters | | Size/area | FPGA are contains lots of LUTs, and routing channels which are connected via bit streams(program). As they are made for general purpose and because of re-usability. They are in-general larger designs than corresponding ASIC design. For example, LUT gives you both registered and non-register output, but if we require only non-registered output, then its a waste of having a extra circuitry. In this way ASIC will be smaller in size. | | Speed | ASIC rules out FPGA in terms of speed As ASIC are designed for a specific application they can be optimized to maximum; hence we can have high speed in ASIC designs. ASIC can have height speed locks. | | Cost | FPGAs are cost effective for small applications. But when it comes to complex and large volume designs (like 32-bit processors) ASIC products are cheaper. | | Power | FPGA designs consume more power than ASIC designs. As explained above the unwanted circuitry results wastage of power. FPGA wont allow us to have better power optimization. When it comes to ASIC designs we can optimize them to the fullest. | |